

Anti-parallel Module

Description

- 1) A package consists of two inverse parallel SCR chips, which non-repetitive peak off-state voltage is up to 2000V
- 2) Welding by vacuum welding technology, which provide high reliability
- 3) Insulated by silicone gel, provide a insulation voltage of 3000V~



Typical Application

Soft start, solid state relay, AC/DC switch, temperature control.

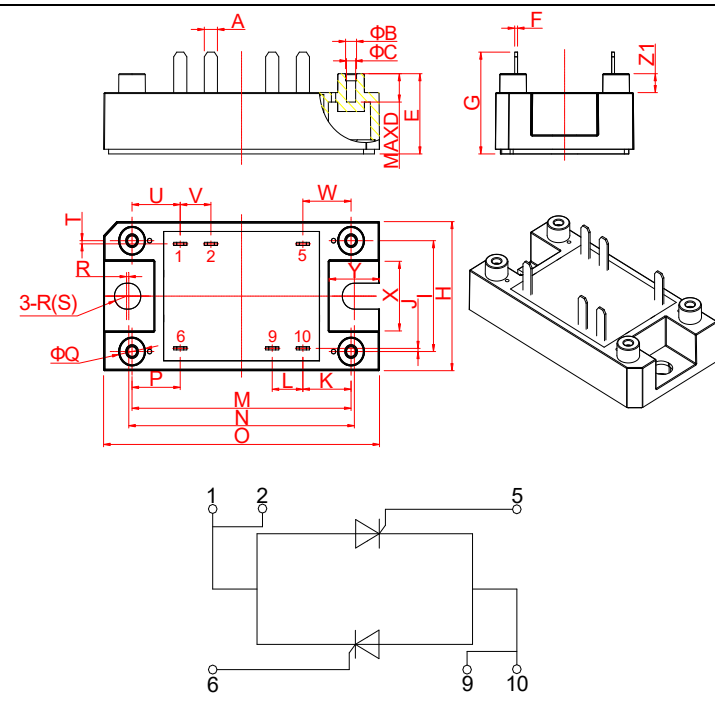
Absolute Maximum Ratings (Packaged into V1-A-Pack, unless otherwise specified, $T_{CASE}=25^{\circ}C$)

Parameter	Test Conditions	Symbol	Values			Unit
			12	16	18	
Operating junction temperature range		T_j	-40-125			$^{\circ}C$
Storage temperature range		T_{stg}	-40-125			$^{\circ}C$
Repetitive peak off-state voltage	$T_j=25^{\circ}C$	V_{DRM}	1200	1600	1800	V
Repetitive peak reverse voltage	$T_j=25^{\circ}C$	V_{RRM}	1200	1600	1800	V
Non-repetitive peak off-state voltage	$T_j=25^{\circ}C$	V_{DSM}	1300	1700	1900	V
Non-repetitive peak reverse voltage	$T_j=25^{\circ}C$	V_{RSM}	1300	1700	1900	V
RMS on-state current	$T_C=85^{\circ}C$	$I_{T(RMS)}$	150			A
Peak on-state surge current	$t_p=10ms V_R=0.6V_{RRM}$	I_{TSM}	2200			A
I^2t value for fusing	$t_p=10ms V_R=0.6V_{RRM}$	I^2t	24200			A^2s
Critical rate of rise of on-state current	$I_G=2 \times I_{GT}$	di/dt	150			$A/\mu s$
Insulation voltage	A.C 50Hz(1s/1min)	V_{ISO}	3600/3000			V

Electrical Characteristics (Packaged into V1-A-Pack, unless otherwise specified, $T_{CASE}=25^{\circ}C$)

Parameter	Test Conditions	Symbol	Values	Unit
Peak on-state voltage	$I_T=300A$ $t_p=380\mu s$	V_{TM}	≤ 1.8	V
Threshold voltage	$T_j=125^{\circ}C$	V_{TO}	≤ 0.9	V
Dynamic resistance	$T_j=125^{\circ}C$	R_d	≤ 2.1	m Ω
Repetitive peak off-state current	$V_D=V_{RRM}$ $T_C=25^{\circ}C$	I_{DRM1}	≤ 100	μA
	$T_C=125^{\circ}C$	I_{DRM2}	≤ 30	mA
Repetitive peak reverse current	$V_R=V_{RRM}$ $T_C=25^{\circ}C$	I_{RRM1}	≤ 100	μA
	$T_C=125^{\circ}C$	I_{RRM2}	≤ 30	mA
Triggering gate current	$V_D=12V$ $R_L=30\Omega$	I_{GT}	20-120	mA
Holding current	$I_T=1A$	I_H	≤ 250	mA
Latching current	$I_G=1.2 I_{GT}$	I_L	≤ 300	mA
Triggering gate voltage	$V_D=12V$ $R_L=30\Omega$	V_{GT}	≤ 1.8	V
Non triggering gate voltage	$V_D=V_{DRM}$ $T_j=125^{\circ}C$	V_{GD}	≥ 0.25	V
Critical rate of rise of voltage	$V_D=2/3V_{DRM}$ $T_j=125^{\circ}C$ Gate Open	dv/dt	≥ 1000	V/ μs
Thermal resistance	Junction to case	$R_{th(j-c)}$	0.35	$^{\circ}C/W$

Mechanical Characteristics

Module size	63x31.6mm																																																																																																																																																																																																									
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Performance Curves

FIG.1: Forward characteristics(per thyristor)

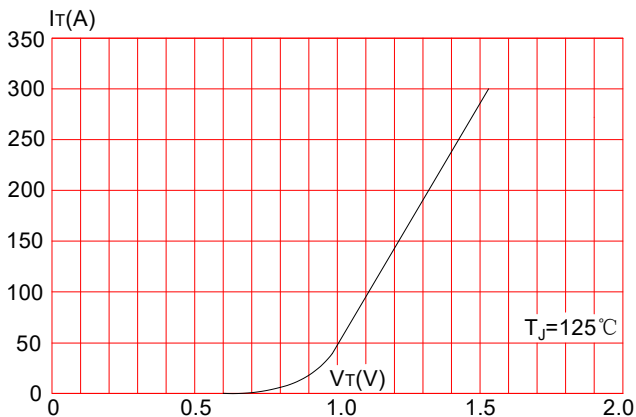


FIG.2: Surge overload current vs. time

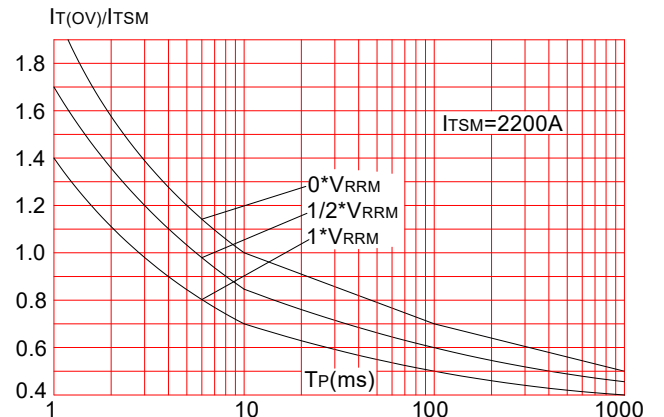


FIG.3: Power dissipation per module vs. R.M.S. current

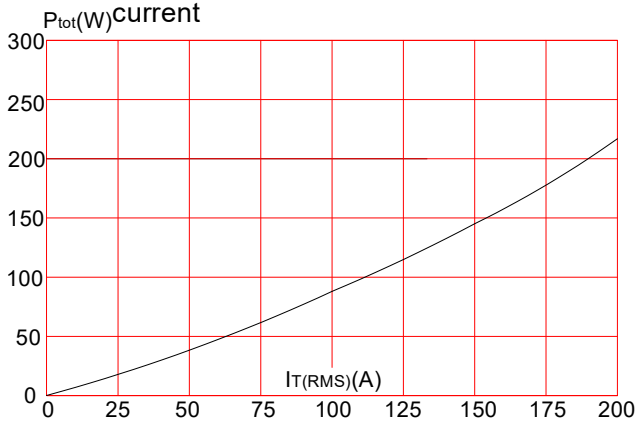
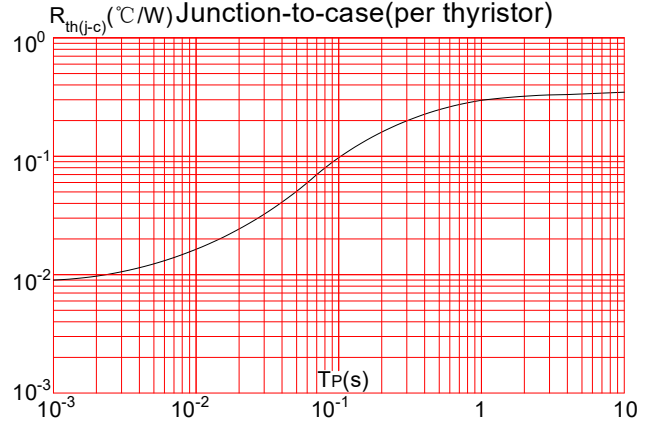


FIG.4: Maximum transient thermal impedance Junction-to-case(per thyristor)



Ordering Information

